DETAILED ACTION

1. This Office Action is in regards to the most recent papers filed on 12/31/2009.

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/31/2009 has been entered.

Non-Compliant Amendments

3. As noted in the Notice of Non-Compliance issued 11/23/2009, in response to the amendments after final submitted 11/2/2009, claim 1 indicates that the word "travel" was previously present, and was removed in favor of the word "interval." However, the word "travel" was never present. However, as it is apparent that Applicant intended the original word "interval" to be present in the instant claims, for purposes of expedited prosecution, the claims have been considered, as detailed below.

Response to Arguments

4. Applicant's arguments filed 12/31/2009 have been fully considered but they are not persuasive.

5. The arguments provided by Applicant appear to focus on the newly amended claimed subject matter. As such, the rational for maintaining the rejection under 35 USC 103(a) is provided below.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-10, 12-15, and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher in US Patent 6,434,620, hereafter referred to as "Boucher" in view of "Introduction to the Remote Monitoring (RMON) family of MIB Modules" by Waldbusser, Cole, Kalbfleisch, and Romascanu, hereafter referred to as "Waldbusser" and Kraslavsky in US 5,699,350, hereafter referred to as "Kraslavsky."

8. With regard to claim 1, Boucher discloses a network interface comprising:

a direct memory access unit (Boucher: Column 8, lines 32-38);

a network data transmit path to couple a host system to a network (Boucher: Column 2, lines 28-42. The disclosure is towards an intelligent network interface card, which is an interface between a host system and a network.); and

circuitry to:

receive and transmit network data for a host processor of the host system, the transmitting network data via the network data transmit path (Boucher: Abstract. The network data is between the host system and the network, meaning it is for a host processor of that system, and is performed via the network data transmit path.);

intercept from the network data transmit path one or more packets from said host processor (Boucher: Column 44, lines 20-32. The INIC maintains statistics, and is the only source of certain statistics. Thus, it is clear that the INIC collects the statistics, and thus intercepts the packets to collect the information.);

generate, based on the receiving and transmitting network data, a set of statistics metering operation of the network interface (Boucher: Column 44, lines 20-23), the set of statistics includes at least one selected from the group of (1) a number of bytes received, and (2) a number of packets received (Boucher: Column 56, lines 51-63); and

initiate direct memory access transfers of the set of statistics from the network interface to a memory of the host system accessible by the host processor (Boucher: Column 63, lines 17-43 and Column 56, lines 27-33. Any transfer of data between a source and a destination, where the data is to be utilized for some purpose, will be placed in some sort of memory, whether the memory is a cache, register, RAM, or non-volatile storage.).

Boucher does not disclose expressly that that the circuitry periodically initiates the direct memory access transfers at a periodicity of a time interval value, or that the circuitry configures said initiation of the direct memory access transfers using a configuration information, wherein the circuitry to determine said configuration information from a payload of said one or more packets, wherein said configuration information comprises said time interval value.

However, Waldbusser discloses the Remote Monitoring family of MIB modules. The functions described in Waldbusser includes the tpmAggregateReportsGroup, which is used to provide the collection of aggregated statistical measurements for the configured report intervals (Waldbusser: Page 16, Section 4.11, "The tpmAggregateReportsGroup"). Further, the statistics are over an interval specified by the management station (Waldbusser: Page 7, paragraph 2).

It would have been obvious to combine Waldbusser with the disclosure of Boucher.

The suggestion/motivation for doing so would have been that statistical information on the network interface of Boucher could be collected automatically at certain intervals configured by the management station. This allows a program or user monitoring the interface to receive recent statistics without requiring that the user refresh the statistics report manually.

Further, Waldbusser discloses that it was well known to provide configuration information including a time interval value to the network interface card (Waldbusser:

Page 16, tpmAggregateReports group and Waldbusser: Page 23, section 5.6, paragraph 1).

Thus, it would have been obvious to modify the teachings of Boucher as modified by Waldbusser to provide configuration information including a time interval value to the network interface card.

The suggestion/motivation for doing so would have been that performing the transfer of the statistics was known. It was also known to transfer the statistics based on requests from the host processor (see Boucher: Column 63, lines 17-43 and Column 56, lines 27-33), as admitted by Applicant (Applicant's Specification: Paragraph [0008]). However, this can cause a burden on the system, as the processor would have to manually initiate each transfer of the statistics. By allowing the processor to determine how often to transfer the statistics, the processor would not have to utilize resources to initiate each transfer, instead simply being able to access the most up-to-date statistics when needed.

Further, Kraslavsky teaches a system where a packet is received from a computer device to be forwarded to a LAN, and the network interface detects that the packet is addressed to a predetermined address, and alters the configuration of the network interface in accordance with the configuration of the information in the packet (Kraslavsky: Abstract).

Accordingly, it would have been obvious to utilize the configuration packet of Kraslavsky with the system of Boucher as modified by Waldbusser.

The suggestion/motivation for doing so would have been that utilizing the same communication paths for reconfiguration and network communication allows the hardware to be designed more efficiently, as configuration of the network interface should occur infrequently enough that having a dedicated communication path to configure the network card would be inefficient. Further, utilizing a software reconfiguration as opposed to a hardware reconfiguration scheme (e.g. jumpers) allows the network interface card to be more easily configured to meet the user's requirements without requiring that the system be turned off, then subsequently rebooted to make the configuration changes.

9. With regard to claim 2, Boucher as modified by Walbusser and Kraslavsky teachesthat the set of statistics comprises each of the following: a number of packets received by the interface, a number of bytes received by the interface, a number of packets transmitted by the interface, and a number of bytes transmitted by the interface (Boucher: Column 56, lines 51-63).

10. With regard to claim 3, Boucher as modified by Walbusser and Kraslavsky teachesthe invention as substantially claimed except that the circuitry comprises circuitry to include a timestamp with the direct memory access transfer of the set of statistics, the timestamp being a time when the values of the set of statistics transferred by direct memory access were set by the network interface.

However, Official Notice is taken that it was well known to have timestamps indicating when data was written. For example, it was well known with operating systems to include a timestamp indicating when a file was last modified and when the file was created.

Accordingly, it would have been obvious to modify the teachings of Boucher as modified by Waldbusser to include a timestamp with the direct memory access transfer of the set of statistics, the timestamp being a time when the values of the set of statistics transferred by direct memory access were set by the network interface.

The suggestion/motivation for doing so would have been that including information on when the set of statistics were set allows the system to be aware of the time that the set of statistics were current, which is valuable for purposes of analysis of the conditions of the connection. For example, a large number of packets received may be evidence of a DoS attack, where having knowledge of the timing would allow the attack to be correlated with other possible attacks, or at the very least analyzed with respect to other known network conditions in order to determine the source of the attack.

11. With regard to claim 4, Boucher as modified by Walbusser and Kraslavsky teachesthat the circuitry to include a sequence count with the direct memory access transfers of the at least one statistic (Boucher: Column 57, lines 6-12).

Boucher does not disclose expressly that the sequence count sequentially numbering successively DMA-ed sets of the statistics.

However, it would have been obvious to have the sequence count sequentially numbering successively DMA-ed sets of the statistics.

The suggestion/motivation for doing so would have been that counters typically sequentially number the events that the counter is associated with. Therefore, a person of ordinary skill in the art would most likely have used sequential numbers to count the transfer of the DMA transmissions of the statistics.

12. With regard to claim 5, Boucher as modified by Walbusser and Kraslavsky teachesthe invention as substantially claimed except that the set of statistics comprises multiple RMON (Remote Monitoring) statistics.

However, Waldbusser discloses RMON, and the collection of statistics within RMON (Waldbusser: Page 3, section 3).

It would have been obvious to combine the teachings of Waldbusser with the combination of Waldbusser and Boucher.

The suggestion/motivation for doing so would have been RMON, as in Waldbusser, allows for monitoring devices to be utilized to remotely monitor a network. Any statistic that is collected within the RMON framework would result in the statistic being an RMON statistic as claimed.

13. With regard to claim 6, Boucher as modified by Walbusser and Kraslavsky teachesthat the circuitry comprises circuitry to initiate direct memory access transfer of received network data (Boucher: Column 8, lines 30-37).

14. With regard to claim 7, Boucher as modified by Walbusser and Kraslavsky teachesthat the network interface comprises a framer (Boucher: Column 56, lines 18-26).

15. With regard claim 8, Boucher as modified by Walbusser and Kraslavsky teaches that the network interface comprises a Media Access Controller (MAC) (Boucher: Figure 21, MAC-A to MAC-D).

16. With regard to claim 9, Boucher as modified by Walbusser and Kraslavsky teaches that the network interface comprises a PHY (Boucher: Column 77, lines 6-15).

17. With regard to claim 13, Boucher as modified by Walbusser and Kraslavsky as currently applied teaches the invention as substantially claimed except that the circuitry to configure comprises circuitry to determine from said configuration information a first location in the memory for a first direct memory access transfer and a second location in the memory, different from the first location, for a second direct memory access transfer.

However, for direct memory access transfers, in order to initiate a direct memory access transfer, at least one memory location needs to be provided in some configuration in order to determine where to write the data.

Thus, Official Notice is taken that it would have been well known to provide the information in a configuration information, such as that provided in the teachings of Kraslavsky, to determine where to write the information when the transfer is performed. Further, Official Notice is taken that it would have been well known to provide at least one other location for a subsequent transfer.

The suggestion/motivation for doing so would have been that for statistics, often, the statistics for a single point in time are not of particular use, as trends in the network cannot be determined from a single time. Rather, having an archive of past measurements would allow trends to be determined, thus making the data more useful. Accordingly, in the interests of archiving information, the mechanism for acquiring the data needs to have a mechanism to not write over the previous data. Either a processor in the host would have to copy the data from the memory location before the next transfer occurs, or different memory locations would have to be provided for each set of statistics. In the first case, the processor would have to perform operations in order to transfer the information each time, which would produce undue burden, and allow for a possibility where the processor, due to other tasks, may not transfer the information in time, thus overwriting the older data. However, if multiple locations are provided, either the processor would have more time to transfer the data, as there would essentially be a buffer for the data, or each final location for the data may be provided, thus allowing the transfer itself to provide for the archiving of data. Further, in situations where multiple locations are provided for, utilizing the mechanism for configuring the transfer, such as taught in Kraslavsky, would allow the system to provide

new memory locations periodically, either based on the system needing the old memory location for other data, or based on the old memory locations being utilized for the archival data, thus preventing overwriting of the archival data.

18. With regard to claim 14, Boucher as modified by Walbusser and Kraslavsky teaches that the circuitry to periodically initiate direct memory access transfers comprises circuitry to:

initiate the first direct memory access based on the first location, the first direct memory access transfer to transfer to the first location data indicating a first value of a statistic at a first time (As detailed in the rejection of claim 13, the multiple locations are provided for archival purposes. Thus, this limitation is rejected for substantially similar reasons as provided for claim 13.); and

initiate, after the first direct memory access transfer, the second direct memory access transfer based on the determining the second location, the second direct memory access transfer to transfer to the second location data indicating a second value of the statistic at the second time (As detailed in the rejection of claim 13, the multiple locations are provided for archival purposes. Thus, this limitation is rejected for substantially similar reasons as provided for claim 13. Further, as detailed in the rejection of claim 13, these would be performed according to the times.).

19. With regard to claim 15, Boucher as modified by Walbusser and Kraslavsky teaches that the direct memory access unit comprises circuitry to notify a processor of completion of the transfer (Boucher: Column 90, line 64 to column 91, line 12).

20. With regard to claim 39, Boucher as modified by Waldbusser and Kraslavsky teaches the invention as substantially claimed except that the memory of the host system comprises a ring including the first location and the second location, the ring to store snapshots to counter values of the network interface.

However, Official Notice is taken that it was well known in the art to provide for a ring, cyclic, or circular buffer in memory. A ring buffer is a buffer in which n memory locations are provided for writing information, where a first data is written in the first memory location, a second data is written to the second memory location, and so on until the nth data is written to the nth memory location. Then the next data (n+1) is written over the data in the first memory location, where the cycle begins again. Thus, a ring buffer is also an example of a FIFO buffer, where the first data in is the first data out (overwritten).

Thus, it would have been obvious to utilize a ring buffer with the teachings of Boucher as modified by Walbusser and Kraslavsky.

The suggestion/motivation for doing so would have been that as detailed in the rejection of claim 13, performing a data transfer each and every time a DMA operation is performed from the location that the DMA transfer wrote the data to would produce undue burden on the processor, and increases the likelihood of losing data, as if the

processor is busy for the time period between transfers, and does not get the chance to transfer the information from the write location, then the data may be lost. By providing multiple locations for the data to be written, the processor would have more time to archive the data before it is lost. Further, in situations where the processor is not copying the data for archival purposes, but rather the DMA transfer writes the information directly to the archived locations, this would allow a finite number of locations to be utilized for the statistics, thus ensuring that the storage resources of the system are not burdened by archiving the statistics. Rather, a certain number of statistics can be stored for review, where the number would be enough to see a trend in the statistics, where when the allocated spaces are filled, the oldest statistics are overwritten by the new statistics, thus providing for a sliding window of times to view the statistics, which would allow for the system to be configured to utilize the least amount of memory for the number of times that would be required.

21. With regard to claim 40, Boucher as modified by Waldbusser and Kraslavsky teaches the invention as substantially claimed except that the first location is appended to a linked list after the first direct memory access transfer, and wherein the second location is appended to the linked list after the second direct memory access transfer.

However, Official Notice is taken that linked lists were well known in the art. A dynamic linked list is a data structure of pointers, where each node in the linked list includes at least some data and one pointer. The data is the element or elements that are being stored in the list. The pointer would point to the next node. When accessing

the linked list, one of the nodes is read, and the data can be read from the data field of the node. Then, when the next node is desired, the address is retrieved from the second field of the node, the pointer, which gives the memory location of the next node.

Thus, it would have been obvious to utilize linked lists in the teachings of Boucher as modified by Waldbusser and Kraslavsky.

The suggestion/motivation for doing so would have been that as detailed in the rejections of claims 39, 14, and 13, providing for multiple storage locations has many benefits for the system. Within memory, there are several possible ways to store the information. First, the memory locations can be sequential, where a certain number of bits are utilized to represent each statistic, and a certain number of statistics are part of each time. Thus, as long as the system has knowledge of the first memory location, the system can determine where each subsequent location is by counting through the bits. Second, the memory locations can be held in some sort of table, where in order to access a memory location, the system would refer to the table to retrieve the address of the desired memory location. Finally, a linked list type structure would require that the processor has knowledge of at least one node (usually the first, but in some cases, such as doubly-linked lists or circular linked lists, any node in the linked list would suffice), but from that single node, a processor can traverse the linked list to find any data stored in the list. Linked lists are particularly useful in situations where the number of elements in the list may be consistently modified (e.g. adding elements or deleting elements). In a case where the information is all being archived, a linked list would allow nodes, and

thus statistics from certain times, to be continuously added, only limited by the amount of memory available.

22. With regard to claim 41, Boucher as modified by Waldbusser and Kraslavsky teaches that the circuitry to determine said configuration information from the payload of said one or more packets includes circuitry to identify information in the one or more packets indicating that the one or more packets are not to be transmitted over the network (Kraslavsky: Abstract and Figure 10. First, it is noted that there is no requirement of what the source of the packet is. Thus, this limitation is met simply by receiving packets, as the circuitry would determine that any inbound packets are not to be transmitted over the network, but rather are to be sent through the system. Further, Kraslavsky checks the packet's destination address, and if the packet has the address of the network interface card, the packet is held by the network interface card for further processing.).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Christensen whose telephone number is (571)270-1144. The examiner can normally be reached on Monday through Thursday 6:30AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Vaughn can be reached on (571) 272-3922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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